EAST Search History

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	(process produc$4 lead$1frame configur $4 fit$6 semiconductor chip encapsulat$4 plastic compound interlayer attack$5 etchant individual layer surface matrix island remain$4 uniform height void extend$4). clm.	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 12:52
L2	1	(process produc$4 lead$1frame configur $4 fit$6 semiconductor chip encapsulat$4 plastic compound interlayer attack$5 etchant individual layer surface matrix island remain$4 uniform height void extend$4)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 12:53
L3	1	(lead$1frame configur $4 semiconductor chip encapsulat$4 plastic compound interlayer attack$5 etchant individual layer surface matrix island remain$4 uniform height void extend$4)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 12:53

L5	1	(lead$1frame semiconductor encapsulat$4 plastic compound interlayer attack$5 etchant individual layer surface matrix island remain$4 uniform height void extend$4)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 12:54
L6	1	(lead$1frame semiconductor encapsulat$4 plastic compound interlayer etchant individual layer surface matrix island remain$4 uniform height void extend$4)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 12:54
L7	1	(lead$1frame semiconductor encapsulat$4 plastic compound interlayer etchant individual layer surface matrix island uniform height void extend$4)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 12:54
L8	1	(lead$1frame semiconductor encapsulat$4 plastic interlayer etchant individual layer surface matrix island uniform height void extend$4)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 12:54
L9	4	(lead$1frame semiconductor encapsulat$4 plastic interlayer etchant individual layer surface matrix island uniform height void)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 12:54
L10	4	(lead$1frame semiconductor encapsulat$4 plastic interlayer etchant layer matrix island uniform height void)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 12:57

L11	4	(lead$1frame semiconductor encapsulat$4 plastic interlayer etchant matrix island uniform height void)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 12:57
L12	4	(lead$1frame semiconductor encapsulat$4 interlayer etchant matrix island uniform height void)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 12:57
L13	4	(lead$1frame semiconductor encapsulat$4 interlayer etchant island uniform height void)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 12:57
L14	4	(lead$1frame encapsulat$4 interlayer etchant island uniform height void)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 12:57
L15	4	(lead$1frame encapsulat$4 interlayer etchant island uniform void)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 12:58
L16	4	(lead$1frame encapsulat$4 etchant island uniform void)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 12:58
L17	4	(lead$1frame encapsulat$4 etchant island void)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 12:58
L18	338	(lead$1frame encapsulat$4 etchant)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 12:58
L19	26	(lead$1frame encapsulat$4 etchant island)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 12:59
L20	309	18 "257".clas.	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 12:59

L21	154	18 "438".clas.	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 12:59
L22	1	(lead$1frame encapsulat$4 etchant island).clm.	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 13:00
L23	9	(lead$1frame encapsulat$4 etchant).clm.	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 13:00
L24	61	(lead$1frame encapsulat$4 etchant void)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 13:01
L25	1	(lead$1frame encapsulat$4 etchant void).clm.	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 13:01
L26	51	24 "257".clas.	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 13:02
L27	24	24 "438".clas.	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 13:03
L28	1	(produc$4 semiconductor leadframe base body interlayer attack$6 etchant layers surface matrix island uniform height void chip plastic compound encapsulating hous $4).clm.	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 13:08
L29	4	(semiconductor leadframe interlayer attack$6 etchant layers surface matrix island uniform height void chip plastic compound encapsulating hous $4)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 13:09

L30	4	(semiconductor leadframe interlayer attack$6 etchant layers surface matrix island void chip plastic compound encapsulating hous $4)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 13:09
L31	4	(semiconductor leadframe interlayer attack$6 etchant layers surface matrix island void chip plastic encapsulat$4 hous$4)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 13:09
L32	4	(semiconductor leadframe interlayer etchant layers surface matrix island void chip plastic encapsulat $4 hous$4)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 13:09
L33	4	(leadframe interlayer etchant layers matrix island void chip plastic encapsulat$4 hous$4)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 13:10
L34	4	(leadframe interlayer etchant island void chip plastic encapsulat $4 hous$4)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 13:10
L35	4	(leadframe interlayer etchant island void encapsulat$4 hous$4)	US-PGPUB; USPAT; UPAD	AND	ON	2009/10/20 13:10

10/20/2009 1:12:48 PM
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